ABSTRACT OF THE DISCLOSURE

There is provided a MISFET which suppresses a short-channel effect in a deep submicron region and has a low parasitic resistance, a low parasitic capacitance, and a small drain junction leakage current. A shallow concave is formed in a channel forming portion and an extension region forming portion of a MISFET, shallow ion implantation for forming an extension region is performed to a bottom surface of the shallow concave. Deep ion implantation for forming a source/drain region is performed to a silicon substrate adjacent to the concave, and the position of a peak concentration of the shallow ion implantation is caused to coincide with the position of a peak concentration of the deep ion implantation, so that a MISFET which suppresses a short-channel effect and has a low source/drain parasitic resistance, a low source/drain parasitic capacitance, and a small drain junction leakage current generated by SALICIDE steps can be provided. The MISFET according to the invention is preferably used as a means for providing a semiconductor substrate constituted by a high-speed CMOS circuit having a high integration level at a high yield and high reliability.